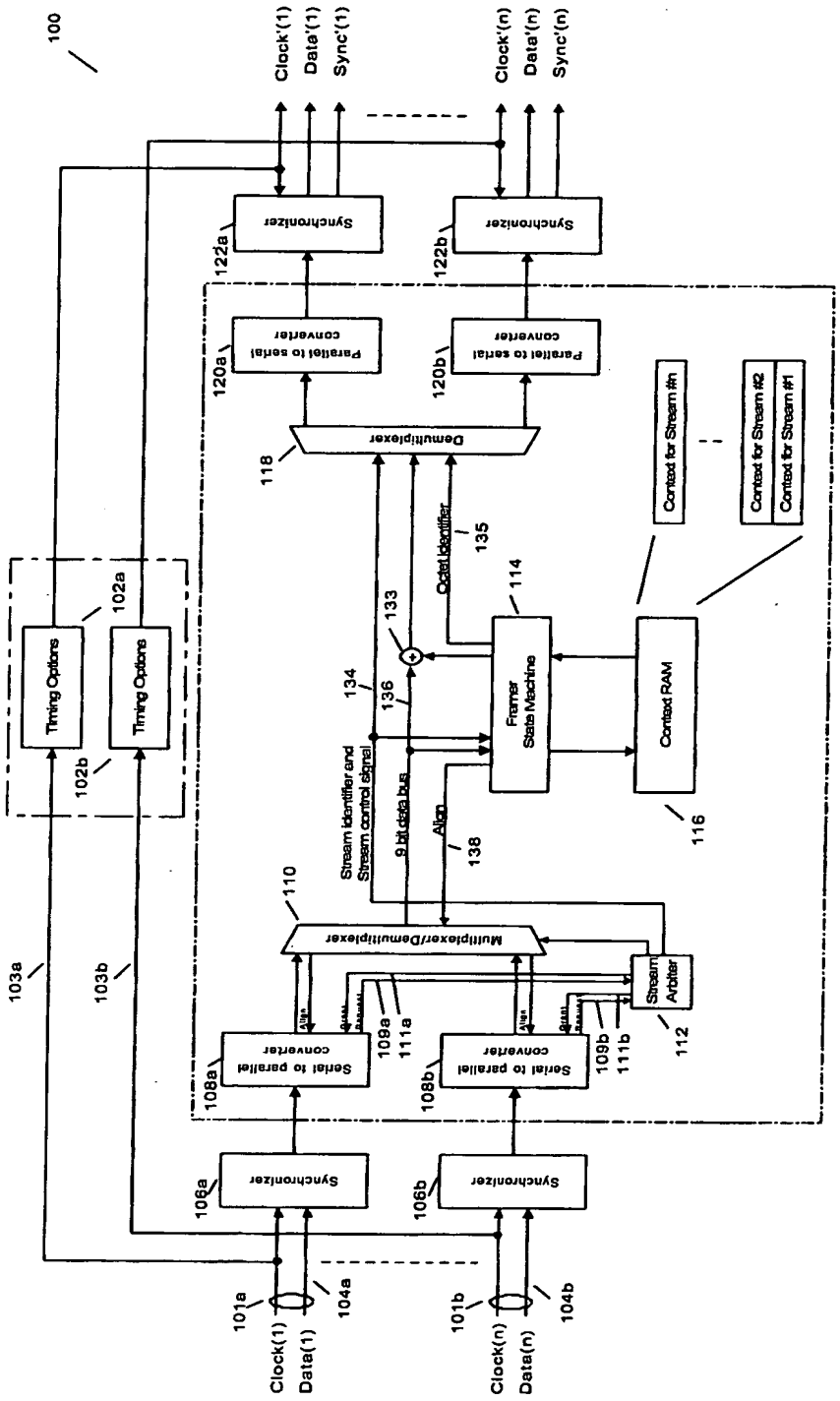
100
Clock'(1)
Data'(1)
Sync'(1)
Clock'(n)
Data'(n)
Sync'(n)
Synchronizer
122a
122b
Parallel to serial converter
120a
120b
Demultiplexer
118
Octet Identifier
135
Context for Stream #n
Context for Stream #2
Context for Stream #1
114
133
134
136
Framer State Machine
Context RAM
116
Timing Options
102a
102b
Stream Identifier and Stream control signal
9 bit data bus
Align
138
110
Multiplexer/Demultiplexer
Stream Arbiter
112
Serial to parallel converter
108a
108b
109a
111a
109b
111b
106a
106b
103a
103b
101a
101b
104a
104b
Clock(1)
Data(1)
Clock(n)
Data(n)

FIG. 1

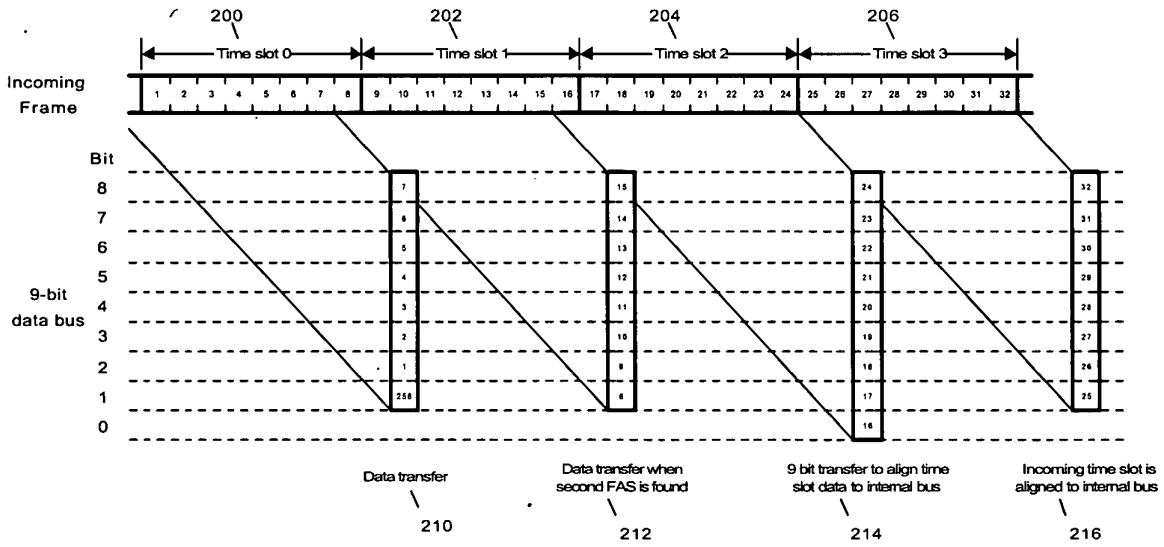
200
202
204
206
Time slot 0
Time slot 1
Time slot 2
Time slot 3
Incoming Frame
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
Bit
8
7
6
5
4
3
2
1
0
9-bit data bus
Data transfer
210
Data transfer when second FAS is found
212
9 bit transfer to align time slot data to internal bus
214
Incoming time slot is aligned to internal bus
216

FIG. 2

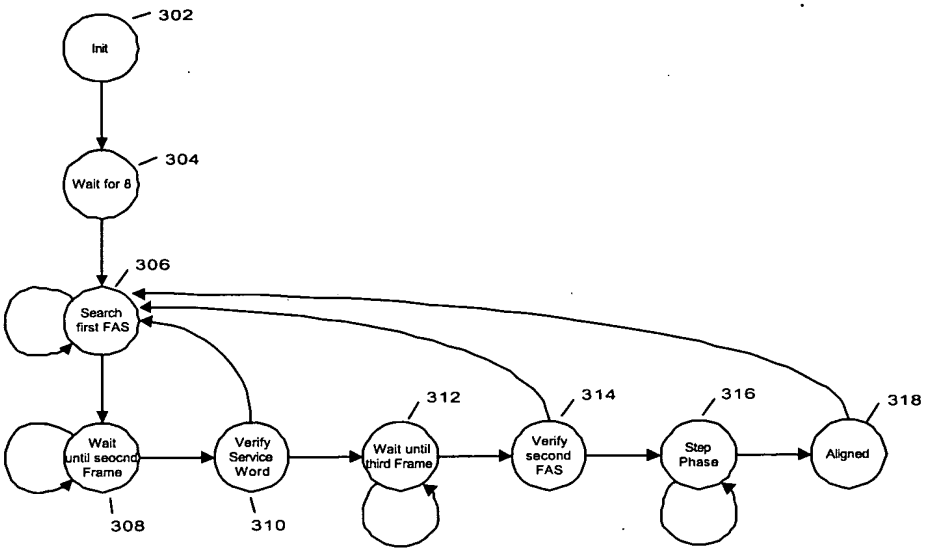
302
Init
304
Wait for 8
306
Search first FAS
Wait until seocnd Frame
308
Verify Service Word
310
312
Wait until third Frame
314
Verify second FAS
316
Step Phase
318
Aligned

Figure 3